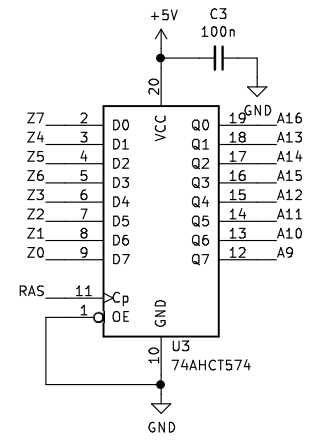
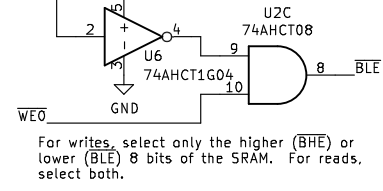
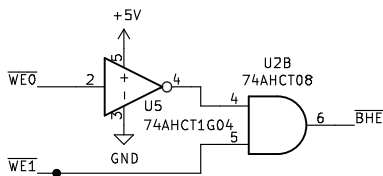
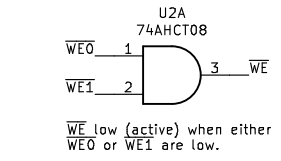
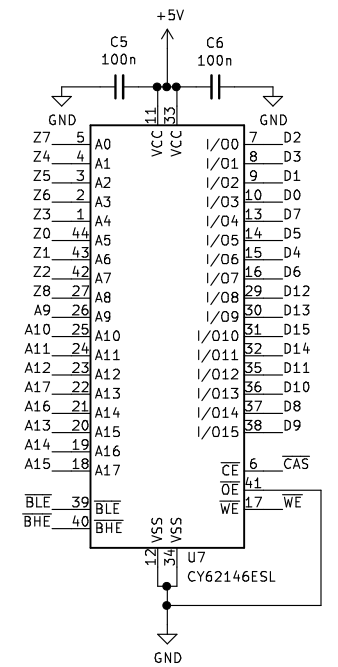
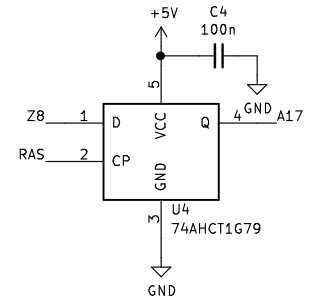


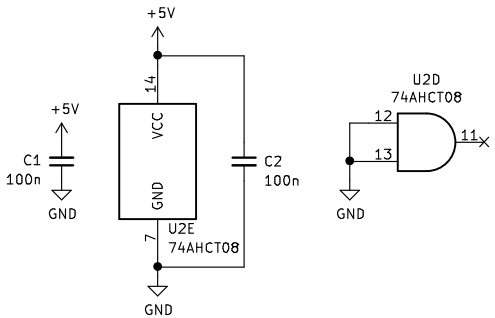
Latches are positive clocked, so invert the RAS signal.



Latch row addresses to SRAM.



256K x 16bit SRAM with high/low 8-bit selects.



Teipen Mwncl	
Sheet: /	
File: cc3-512k.sch	
Title: CoCo3 512K SRAM	
Size: A4	Date: 2021-03-13
KiCad E.D.A. kicad 5.1.9+dfsg1-1	Rev: TM009/1
	Id: 1/1